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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,906	07/31/2003	Li-Yi Chen	SUND 470	9613

23995 7590 06/02/2006

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EXAMINER

LIANG, REGINA

ART UNIT	PAPER NUMBER
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2629

DATE MAILED: 06/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,906	CHEN, LI-YI	
	Examiner	Art Unit	
	Regina Liang	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 March 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1, 2, 4-17 and 19-34 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 2, 4-17, 19-34 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This Office Action is response to amendment filed 3/13/06. Claims 1, 2, 4-17, 19-34 are currently pending in the application.
2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

3. Claims 1, 2, 4-17, 19-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishihara in view of Nishihara (US. PA.T NO. 6,014,126) in view of Ham (US 2002/0196224).

As to claims 1, 15, Figs. 1 and 5 of Nishihara discloses a method of frame processing in which a plurality of frames are sequentially fed into a frame processing device (frequency converting circuit 2) at a first refresh rate (first frame frequency S2), wherein the frame processing device controls a refresh rate of the frames to be displayed in a display device, the method comprising the steps of: inputting a first input frame; inputting a second input frame (the display data having a plurality of frames sequentially fed into the frame memory 4 frame by frame, it is inherent the display data including first input frame and second input frame, the second input frame is inputted after the first input frame); determining a plurality of corresponding output frames according to the first and second input frames, wherein the second input frame is input into the frame processing device after the first input frame is input; and outputting the output frames sequentially from the frame processing device at a second refresh rate (second frame frequency S7; see col. 6, lines 36-49, col. 7, lines 58-64 for example).

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Nishihara also teaches the second refresh rate is greater than the first refresh rate (the second frame frequency is higher than or faster than the first frame frequency).

Nishihara does not disclose determining the output frames with respect to difference in pixel data between the first and second input frames to increase pixel response rate.

However, Ham teaches a display device using a high-speed driving scheme to increase the pixel response rate ([0008]). Table 1 on page 1 of Ham teaches determining a plurality of corresponding output frames according to the first and second input frames with respect to difference in pixel data between the first and second input frames (as shown in the Table 1, the input data voltage is modulated (output frames) to be greater when the data voltage VD_n inputted at the current frame F_n is larger than the data voltage VD_{n-1} of the previous frame F_{n-1} , and the data voltage (output frames) is modulated to be smaller when the data voltage inputted at the current frame F_n is smaller than the data voltage of the previous frame, and see [0013]-[0015]). Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the teachings of Nishihara and Ham so as to provide a LCD employing a high-speed driving scheme reduces a motion-blurring phenomenon in a moving picture, thereby displaying a picture with desired color and brightness ([0009] of Ham).

As to claim 2, Ham teaches using a look-up table to pre-set the relationship among the input frames and the corresponding output frames (modulated data voltage) with respect to difference in pixel data between the first and second input frames (see Table 1 on page 1 and Table 2 on page 4).

As to claims 4, 19, Nishihara teaches the second frame frequency is a multiple of the first frame frequency (col. 6, lines 42-44).

As to claims 13, 28, Nishihara teaches the display device (10b) is a LCD panel.

As to claims 14, 29, Nishihara teaches the relationship among the input frames and the corresponding output frames is determined (set by the clock generating unit) by the physical properties of the LCD panel, the luminance of the LCD panel, and the brightness perceived by unman eyes (col. 7, lines 58-65).

As to claims 5, 20, Table 1 on page 1 of Ham teaches the first input frame (previous frame F_{n-1}), second input frame (current frame F_n) and the output frames (modulated data voltages) having first pixel datum, second pixel datum, and output pixel datum, respectively. Table 1 of Ham also teaches the output frames include an overdrive output frame and the overdrive output frame includes an output pixel datum which is greater than the second pixel datum.

As to claims 6, 10, 21, 25, Ham teaches overdrive output frame outputted from the frame processing device.

As to claims 8, 9, 12, 23, 24, 27, Table 1 of Ham teaches the output frames having an overdrive compensation output frame which is output from the frame processing device and including a pixel data that is smaller than the second pixel ([0014] of Ham states “the data voltage VD_n inputted at the current frame F_n is smaller than the data voltage VD_{n-1} of the previous frame F_{n-1} as a result of such a comparison, it is modulated to be smaller”).

As to claims 7, 22, Ham teaches using overdrive voltages to increase data voltage applied to the pixel according to the output pixel datum is greater than the second pixel datum. Thus, Nishihara as modified by Han would have display luminosity of a pixel of the display device according to the output pixel datum is greater than the display luminosity of the pixel according

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to the second pixel datum as claimed so as to provide an uniform pixel luminosity over the entire display.

As to claims 11, 26, Han teaches using overdrive voltages to reduce data voltage applied to the pixel according to the output pixel datum is less than the second pixel datum. Thus, Nishihara as modified by Ham having display luminosity of a pixel of the display device according to the output pixel datum is less than the display luminosity of the pixel according to the second pixel datum as claimed so as to provide uniform pixel luminosity over the entire display.

As to claim 16, Fig. 6 of Ham teaches a memory device which stores a lookup table having entries about the relationship among the input frames and output frames (modulated data).

As to claim 17, Fig. 3 of Nishihara teaches the memory device is a RAM (13).

4. Claims 30-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishihara in view of applicant's admitted prior art (Figs. 2A, 2B, and [0005]-[0009] of the specification).

As to claim 30, Figs. 1 and 5 of Nishihara discloses a method of frame processing in which a plurality of frames are sequentially fed into a frame processing device (frequency converting circuit 2) at a first refresh rate (first frame frequency S2), wherein the frame processing device controls a refresh rate of the frames to be displayed in a display device, the method comprising the steps of: inputting a first input frame; inputting a second input frame (the display data having a plurality of frames sequentially fed into the frame memory 4 frame by frame, it is inherent the display data including first input frame and second input frame, the

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second input frame is inputted after the first input frame); determining a plurality of corresponding output frames according to the first and second input frames, wherein the second input frame is input into the frame processing device after the first input frame is input; and outputting the output frames sequentially from the frame processing device at a second refresh rate (second frame frequency S_7 ; see col. 6, lines 36-49, col. 7, lines 58-64 for example).

Nishihara teaches the frequency of the standard clock is set in such a manner that the image data are read out from the frame memory 4 faster than they are written into the memory 4 such that the image data can be read out a number of times from the memory while the image data of the one frame are written into the memory (col. 7, lines 58-65), which reads on the relationship among the input frames and the corresponding output frames with respect to the second refresh rate is pre-stored (pre-set) in the frame processing device.

Nishihara does not disclose the output frames having at least one overdrive output frame. However, applicant's admitted prior art teaches it is well known in the art for driving a display using an overdrive technique (overdrive output frame) to increase the pixel response rate, the overdrive voltage (e.g., V_3) is higher than a voltage (e.g., V_2) which is output from an output frame (see [0006]) of the specification). Thus, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Nishihara to use the overdrive technique as taught by applicant's admitted prior art so as to increase the pixel response rate when the pixel luminosity needs to be increased.

As to claim 31, Nishihara teaches the second frame frequency is a multiple of the first frame frequency (col. 6, lines 42-44).

As to claim 32, applicant's admitted prior art teaches a relationship between the input frames and output frame is determined by the physical properties of the LCD panel, luminance of the LCD panel and the brightness perceived by the human eyes, for example see paragraphs [0007-0008] which discloses the physical properties of the LCD ([0007]-physical arrangement of a LCD panel) affects light transmissivity and luminosity of a pixel as a result thereof, further affects the response time of the LCD panel. The admitted prior art further discloses the slow response time can affect the previous frame and current frame being displayed (see [0008]). Therefore, applicant's admitted prior art discloses that a relationship exists between the input and output frames are determined by the physical properties of the LCD panel.

As to claims 33, 34, Nishihara teaches the output data from the frame memory can be converted into display voltages for driving the LCD display, such that higher output datum (higher voltage) would have a higher luminosity of a pixel, lower output datum (lower voltage) would have a lower luminosity of a pixel.

Response to Arguments

5. Applicant's arguments with respect to claims 1, 2, 4-17, 19-34 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's remarks regarding the combination of Nishihara and applicant's admitted prior art on pages 14-17, 22-23 are not persuasive. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art.

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See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, applicant's admitted prior art teaches "Figs. 2A and 2B show the traditional technique used to increase the pixel response rate, called overdrive" and "In order to increase the response rate, a pixel voltage V3, which is higher than V2, is input when frame f2 is displayed. Pixel voltage V3 is called the overdrive voltage herein" (lines 1-2 and 10-13 in [0009] of applicant's admitted prior art). Therefore, using overdrive voltage to increase pixel response rate is clearly suggested by applicant's admitted prior art and is not proposed by the Examiner as erroneously alleged by the applicant.

Applicant's remarks regarding claim 32 on pages 23-24 are not persuasive. Applicant's admitted prior art teaches a relationship between the input frames and output frame is determined by the physical properties of the LCD panel, luminance of the LCD panel and the brightness perceived by the human eyes, for example see paragraphs [0007-0008] which discloses the physical properties of the LCD ([0007]-physical arrangement of a LCD panel) affects light transmissivity and luminosity of a pixel as a result thereof, further affects the response time of the LCD panel. The admitted prior art further discloses the slow response time can affect the previous frame and current frame being displayed (see [0008]). Therefore, applicant's admitted prior art discloses that a relationship exists between the input and output frames are determined by the physical properties of the LCD panel.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

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Lin et al (US 2003/0137527) teaches an overdrive system and method of operating overdrive system.

Suzuki et al (US 6,894,669) teaches a display control device of LCD.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.


8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Regina Liang whose telephone number is (571) 272-7693. The examiner can normally be reached on Monday-Friday from 8AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached on (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

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may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


Regina Liang
Primary Examiner
Art Unit 2674

5/24/06